# 2M×8 CMOS Synchronous DRAM

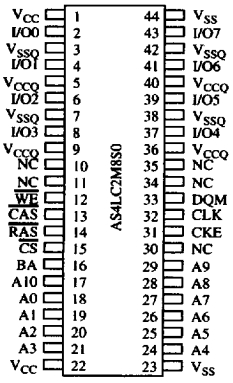
*Advance information*

## Features

- Organization: 1,048,576 words × 8 bits × 2 banks
- All signals referenced to positive edge of clock
- Dual internal banks (controlled by BA)
- High speed
  - 100/83/66 MHz bus speeds
  - 8/10/12 ns clock access time
- Low power consumption
  - Active: 576 mW max
  - Standby: 7.2 mW max, CMOS I/O
- 4096 refresh cycles, 64 ms refresh interval
- Auto refresh and self refresh
- Automatic and direct precharge
- Burst read/write, single write
- Can assert random column address in every cycle
- LVTTL compatible I/O
- 3.3V power supply
- JEDEC standard package, pinout and function
  - 400 mil, 44-pin TSOP type 2
- Read/write data masking
- Programmable burst length (1/2/4/8)
- Programmable burst sequence (sequential/interleaved)
- Programmable $\overline{CAS}$ latency (1/2/3)
- Single write mode
- Latch-up current ≥ 200 mA
- ESD protection ≥ 2000 mA

## Pin arrangement

TSOP




## Pin designation

| Pin(s) | Description |
|---|---|
| DQM | I/O mask |
| A0 to A10 | Address inputs |
| BA | Bank address |
| I/O0 to I/O7 | Input/output |
| $\overline{RAS}$ | Row address strobe |
| $\overline{CAS}$ | Column address strobe |
| $\overline{WE}$ | Write enable |
| $\overline{CS}$ | Chip select |
| $V_{CC}$, $V_{CCQ}$ | Power (3.3V ± 0.3V) |
| $V_{SS}$, $V_{SSQ}$ | Ground |
| CLK | Clock input |
| CKE | Clock enable |

## Selection guide

| | Symbol | 4LC2M8S0-10 | 4LC2M8S0-12 | 4LC2M8S0-15 | Unit |
|---|---|---|---|---|---|
| Bus frequency (CL = 3) | $f_{max}$ | 100 | 83.3 | 66.6 | MHz |
| Maximum clock access time (CL = 3) | $t_{AC}$ | 8 | 10 | 12 | ns |
| Minimum input setup time | $t_S$ | 2.5 | 3.0 | 3.0 | ns |
| Minimum input hold time | $t_H$ | 1.0 | 1.5 | 1.5 | ns |
| Minimum row cycle time | $t_{RC}$ | 90 | 100 | 120 | ns |
| Maximum operating current (burst, CL = 3) | $I_{CC1}$ | 160 | 135 | 110 | mA |
| Maximum CMOS standby current, self refresh | $I_{CC6}$ | 2 | 2 | 2 | mA |

## Functional description

The AS4LC2M8S0 is a high performance 16 megabit CMOS Synchronous Dynamic Random Access Memory (SDRAM) organized as 1,048,576 words × 8 bits × 2 banks. Very high bandwidth is achieved using a pipelined architecture where all inputs and outputs are referenced to the rising edge of a common clock. Programmable burst mode can be used to read up to 8 bytes of data without selecting a new column address. Burst mode allows an 8-bit data word to be output during each clock cycle for a peak data bandwidth of 528 megabits per second at 66 MHz.

The AS4LC2M8S0 also includes two internal banks that can be alternately accessed (read or write) at the maximum clock frequency for seamless interleaving operations. This provides a significant advantage over asynchronous EDO and fast page mode devices.

This SDRAM product also features a programmable mode register, allowing users to select read latency as well as burst length and type (sequential or interleaved). Lower latency improves first data data access in terms of CLK cycles, while higher latency improves maximum frequency of operation. This feature enables flexible performance optimization for a variety of applications.

DRAM commands and functions are decoded from control inputs. Basic commands are as follows:

- Mode register set
- De-activate bank
- Deactivate all banks
- Select row, activate bank
- Select column, write
- Select column, read
- Deselect, power down
- CBR refresh
- Auto precharge with read/write
- Self refresh

The AS4LC2M8S0 is available in 44-pin plastic TSOP type 2 package and operates with a power supply of 3.3V ± 0.3V. Multiple power and ground pins are provided for low switching noise and EMI. Inputs and outputs are LVTTL compatible.

## Logic block diagram